Claims

1. Control unit for activating an occupant protection means in a motor vehicle,
comprising a first arithmetic unit (R1) and a second arithmetic unit (R2), as well as an activating unit (AE), wherein the first arithmetic unit (R1), the second arithmetic unit (R2) and the activating unit (AE) are respectively clocked asynchronously relative to one another,
characterized in that
- the control unit comprises a first and a second logical AND gate (AND1, AND2),
- the first arithmetic unit (R1) of the control unit has a first pulse count comparator unit (PZVE1) and a first resetter (RES1),
- the second arithmetic unit (R2) of the control unit has a second pulse count comparator unit (PZVE2) and a second resetter (RES2),
- both the clock signal (clk1) of the first arithmetic unit (R1) and the clock signal (clk3) of the activating unit (AE) are fed to the first logical AND gate (AND1) on the input side,
- an output (clkl3) of the first logical AND gate (AND1) is connected to an input of the second pulse count comparator unit (PZVE2),
- an output of the second pulse count comparator unit (PZVE2) is connected to an input of the second resetter (RES2),
- an output of the second resetter (RES2) is connected directly or indirectly to a reset input (RESET1) of the first arithmetic unit (R1),
and
- both the clock signal (clk2) of the second arithmetic unit (R2) and the clock signal (clk3) of the activating unit (AE)

are fed to the second logical AND gate (AND2) on the input side,

- an output (clk23) of the second logical AND gate (AND2) is connected to an input of the first pulse count comparator unit (PZVE1),

- an output of the first pulse count comparator unit(PZVE1) is connected to an input of the first resetter (RES1),

- an output of the first resetter (RES1) is connected directly or indirectly to a reset input (RESET2) of the second arithmetic unit (R2),

such that

- the first resetter (RES1) resets the second arithmetic unit (R2) by outputting a first reset signal (sr1) if the first pulse count comparator unit (PZVE1) detects an inadmissible number of pulses per unit of time in the output signal of the second AND gate (AND2) and

- the second resetter (RES2) resets the first arithmetic unit (R1) by outputting a second reset signal (sr2) if the second pulse count comparator unit (PZVE2) detects an inadmissible number of pulses per unit of time in the output signal of the first AND gate (AND1).

2. Control unit according to Claim 1,
characterized in that

- the control unit has a first and a second logical OR gate (OR1, OR2),

- an output of the second resetter (RES2) is connected indirectly via the second OR gate (OR2) to the reset input (RESET1) of the first arithmetic unit (R1),

- an output of the first resetter (RES1) is connected indirectly via the first OR gate (OR1) to the reset input (RESET2) of the second arithmetic unit (R2),

such that

- the first resetter (RES1) resets the second arithmetic unit (R2) by outputting a first reset signal (sr1) indirectly via the first OR gate (OR1) if the first pulse count comparator unit (PZVE1) detects an inadmissible number of pulses per unit of time in the output signal (clk23) of the second AND gate (AND2) and

- the second resetter (RES2) resets the first arithmetic unit (R1) by outputting a second reset signal (sr2) indirectly via the second OR gate (OR2) if the second pulse count comparator unit (PZVE2) detects an inadmissible number of pulses per unit of time in the output signal (clk13) of the first AND gate (AND1).

3. Control unit according to Claim 1 or Claim 2, characterized in that

- the first resetter (RES1) and/or the second resetter (RES2) is/are connected directly or indirectly to a reset input(RESETAE) of the activating unit (AE), such that

- the first resetter (RES1) resets the activating unit (AE) by outputting a first activator reset signal (sae1) if the first pulse count comparator unit (PZVE1) detects an inadmissible number of pulses per unit of time in the output signal (clk23) of the second AND gate (AND2) and/or

- the second resetter (RES2) resets the activating unit (AE) by outputting a second activator reset signal (sae2) if the second pulse count comparator unit (PZVE2) detects an inadmissible number of pulses per unit of time in the output signal (clk13) of the first AND gate (AND1).

4. Control unit according to any one of Claims 1 to 3, characterized in that

- the control unit has a third logical AND gate (AND3),

- the clock signal (clk1) of the first arithmetic unit (R1) and the clock signal (clk2) of the second arithmetic unit (R2) are fed to the third logical AND gate (AND3) on the input side,
- the output signal (clk12) of the third logical AND gate (AND3) is connected to both an input of the first pulse count comparator unit (PZVE1) and an input of the second pulse count comparator unit (PZVE2),

such that

- the first resetter (RES1) resets the second arithmetic unit (R2) by outputting a first reset signal (sr1) if the first pulse count comparator unit (PZVE1) detects an inadmissible number of pulses per unit of time in the output signal (clk12) of the third AND gate (AND3) and
- the second resetter (RES2) resets the first arithmetic unit (R1) by outputting a second reset signal (sr2) if the second pulse count comparator unit (PZVE2) detects an inadmissible number of pulses per unit of time in the output signal (clk12) of the third AND gate (AND3).

5. Control unit according to any one of the preceding claims, characterized in that

- a watchdog input of the activating unit (AE1) is connected to a first watchdog output (WD1) of the first arithmetic unit (R1),
- an arithmetic unit resetting output (SAE) of the activating unit is connected directly or indirectly via the second OR gate (OR2) to the reset input (RESET1) of the first arithmetic unit (R1),

such that

- the activating unit (AE) outputs an arithmetic unit resetting signal (sae) directly or indirectly via the second OR gate (OR2) to the reset input (RESET1) of the first arithmetic unit (R1) if the activating unit (AE) receives an inadmissible

watchdog signal (wd1) from the first watchdog output (WD1).

6. Control unit according to any one of the preceding claims, characterized in that

- a signal input of the activating unit (AE) is connected to a second watchdog output (WD2) of the second arithmetic unit (R2),
- the arithmetic unit resetting output (SAE) of the activating unit (AE) is connected directly or indirectly via the first OR gate (OR1) to the reset input (RESET2) of the second arithmetic unit (R2),

such that

the activating unit (AE) outputs the arithmetic unit resetting signal (sae) directly or indirectly via the first OR gate (OR1) to the reset input of the second arithmetic unit (RESET2) if the activating unit (AE) receives an inadmissible second watchdog signal (wd2) from the second watchdog output (WD2).

7. Method for monitoring the proper functioning of a control unit, preferably of a control unit according to any one of Claims 1 to 6

characterized in that

- a first combined signal (clk13) is generated by a first logical operation (AND1) from the two clock signals (clk1, clk3) of a first arithmetic unit (R1) and of an activating unit (AE),
- a second arithmetic unit (R2) counts the number of pulses of the first combined signal (clk13) during a time window,
- the second arithmetic unit (R2) compares the number of pulses counted with a second reference value which is stored in the memory of the second arithmetic unit (R2) and
- the second arithmetic unit (R2) outputs a resetting signal to

a first reset input (RESET1) of the first arithmetic unit (R1) if the number of pulses counted deviates by more than an admissible extent from the second reference value of the memory of the second arithmetic unit (R2).

8. Method according to Claim 7,
characterized in that
- a second combined signal (clk23) is generated by a second logical operation (AND2) from the two clock signals (clk2, clk3) of the second arithmetic unit (R2) and of the activating unit (AE),
- the first arithmetic unit (R1) counts the number of pulses of the second combined signal (clk23) during a time window,
- the first arithmetic unit (R1) compares the number of pulses counted with a first reference value which is stored in the memory of the first arithmetic unit (R1) and
- the first arithmetic unit (R1) outputs a resetting signal to a second reset input (RESET2) of the second arithmetic unit (R2) if the number of pulses counted deviates by more than an admissible extent from the first reference value.

9. Method according to any one of Claims 7 or 8,
characterized in that
- the first arithmetic unit (R1) resets the activating unit (AE) by outputting a first activator reset signal (sae1) if the first arithmetic unit (R1) detects an inadmissible number of pulses per unit of time in the second combined signal (clk23) and/or
- the second arithmetic unit (R2) resets the activating unit (AE) by outputting a second activator reset signal (sae2) if the second arithmetic unit (R2) detects an inadmissible number of pulses per unit of time in the first combined signal (clk13).

10. Method according to any one of Claims 7 to 9, characterized in that

- a third combined signal is generated by a third logical operation (AND3) from the two clock signals (clk1, clk2) of the first arithmetic unit (R1) and of the second arithmetic unit (R2),

- both the first arithmetic unit (R1) and the second arithmetic unit (R2) count the number of pulses of the third combined signal (clk12) during a time window,

- both the first arithmetic unit (R1) and the second arithmetic unit (R2) each compare the number of pulses counted with a reference value which is stored in the memory of the first arithmetic unit (R1) or in the memory of the second arithmetic unit (R2),

- the first arithmetic unit (R1) resets the second arithmetic unit (R2) by outputting a first reset signal (sr1) if the first arithmetic unit (R1) detects, by means of the comparison with the respective reference value, an inadmissible number of pulses per unit of time in the third combined signal (clk12) and

- the second arithmetic unit (R2) resets the first arithmetic unit (R1) by outputting a second reset signal (sr2) if the second arithmetic unit (R2) detects, by means of the comparison with the respective reference value, an inadmissible number of pulses per unit of time in the third combined signal (clk12).

11. Method according to any one of Claims 8 to 10, characterized in that

- a first watchdog signal (wd1) is fed from a first watchdog output (WD1) of the first arithmetic unit (R1) to a first watchdog input (AE1) of the activating unit (AE) and thereupon

- an arithmetic unit resetting output (SAE) of the activating unit (AE) outputs an arithmetic unit resetting signal (sae) to the first reset input (RESET1) of the first arithmetic unit (R1) if the first watchdog signal (wd1) is inadmissible and/or

- a second watchdog signal (wd2) is fed from the second watchdog output (WD2) of the second arithmetic unit (R2) to a second watchdog input (AE2) of the activating unit (AE) and thereupon

- the arithmetic unit resetting output (SAE) of the activating unit (AE) outputs the arithmetic unit resetting signal (sae) to the second reset input (RESET2) of the second arithmetic unit (R2) if the second watchdog signal (wd2) is inadmissible.

12. Method according to any one of Claims 7 to 11, characterized in that
one of the two arithmetic units (R1, R2)of the control unit of an occupant protection system of a motor vehicle deactivates the occupant protection system at least partially after single or multiple resetting of the respective other arithmetic unit (R1, R2) or of the activating unit (AE) and/or displays the malfunctions of the control unit and the at least partial deactivation of the occupant protection means to the vehicle occupant.